

CPLD 3 Specification

64 port G-PON

ASGvOLT64

(GPON OLT)

Version: 1.0

Revision History

Document Rev.	Date	Author	Revision Description	CPLD code version
1.0	8/29/2019		Initial OCP releasee	

3.1. Offset 0x01 CPLD version (Read Only)

Example : version 5.01 then reg 0x2 is 5, reg 0x3 is 1

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x2	CPLD version

3.2. Offset 0x02 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x0	CPLD version

3.3. Offset 0x03 SFP_ABS_1 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	MPL4_SFP50_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 49	MPL4_SFP49_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 48	MPL4_SFP48_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON Port 34	MPL3_SFP47_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 35	MPL3_SFP46_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 38	MPL3_SFP45_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 39	MPL3_SFP44_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 42	MPL3_SFP43_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.4. Offset 0x04 SFP_ABS_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	MASK*MPL4_SF P50_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 49	MASK*MPL4_SF P49_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 48	MASK*MPL4_SF P48_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 34	MASK*MPL3_SF P47_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 35	MASK*MPL3_SF P46_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 38	MASK*MPL3_SF P45_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 39	MASK*MPL3_SF P44_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 42	MASK*MPL3_SF P43_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.5. Offset 0x05 SFP_ABS_2 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	MPL4_SFP58_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 62	MPL4_SFP57_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 63	MPL4_SFP56_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON	MPL4_SFP55_MOD_ABS	R	1	0: SFP transceiver is present

	Port 61				1: SFP transceiver is absent
3	PON Port 60	MPL4_SFP54_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 57	MPL4_SFP53_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 56	MPL4_SFP52_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 53	MPL4_SFP51_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.6. Offset 0x06 SFP_ABS_2 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	MASK*MPL4_SF P58_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 62	MASK*MPL4_SF P57_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 63	MASK*MPL4_SF P56_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 61	MASK*MPL4_SF P55_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 60	MASK*MPL4_SF P54_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 57	MASK*MPL4_SF P53_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 56	MASK*MPL4_SF P52_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 53	MASK*MPL4_SF P51_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.7. Offset 0x07 SFP_ABS_3 (Read Only)

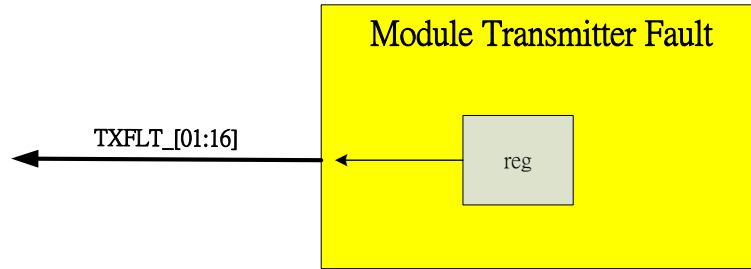
Bit	Front port	Name	R/W	Reset Value	Description
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7:5		Reserved			
4	PON Port 50	MPL4_SFP63_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 51	MPL4_SFP62_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 54	MPL4_SFP61_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 55	MPL4_SFP60_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 58	MPL4_SFP59_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.8. Offset 0x08 SFP_ABS_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	MASK*MPL4_SF P63_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 51	MASK*MPL4_SF P62_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 54	MASK*MPL4_SF P61_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 55	MASK*MPL4_SF P60_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 58	MASK*MPL4_SF P59_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.9. Offset 0x09 TX_Fault_1 (Read only)



The module transmitter fault signal indicates transmitter has detected a fault condition related to laser operation or safety.

Note: LTH7226 XGS-PON transceiver is not supported the TX fault function.

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	MPL4_SFP50_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 49	MPL4_SFP49_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 48	MPL4_SFP48_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 34	MPL4_SFP47_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 35	MPL3_SFP46_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 38	MPL3_SFP45_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 39	MPL3_SFP44_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 42	MPL3_SFP43_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.10. Offset 0x10 TX_Fault_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON	MASK*MPL4_SFP5	R/W	0	1: CPLD passes the Transmit Fault to CPU

	Port 52	0_TX_FAULT			0: CPLD blocks incoming the Transmit Fault
6	PON Port 49	MASK*MPL4_SFP4 9_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	PON Port 48	MASK*MPL4_SFP4 8_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 34	MASK*MPL4_SFP4 7_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 35	MASK*MPL3_SFP4 6_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 38	MASK*MPL3_SFP4 5_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 39	MASK*MPL3_SFP4 4_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 42	MASK*MPL3_SFP4 3_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.11. Offset 0x11 TX_Fault_2 (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	MPL4_SFP58_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 62	MPL4_SFP57_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 63	MPL4_SFP56_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 61	MPL4_SFP55_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 60	MPL4_SFP54_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 57	MPL4_SFP53_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 56	MPL4_SFP52_TX _FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON	MPL4_SFP51_TX	R	1	1: SFP Transmit Fault

	Port 53	_FAULT			0: SFP Transmitter is working well
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3.12. Offset 0x12 TX_Fault_2 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	MASK*MPL4_SFP58 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	PON Port 62	MASK*MPL4_SFP57 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	PON Port 63	MASK*MPL4_SFP56 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 61	MASK*MPL4_SFP55 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 60	MASK*MPL4_SFP54 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 57	MASK*MPL4_SFP53 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 56	MASK*MPL4_SFP52 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 53	MASK*MPL4_SFP51 _TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.13. Offset 0x13 TX_Fault_3 (Read only)

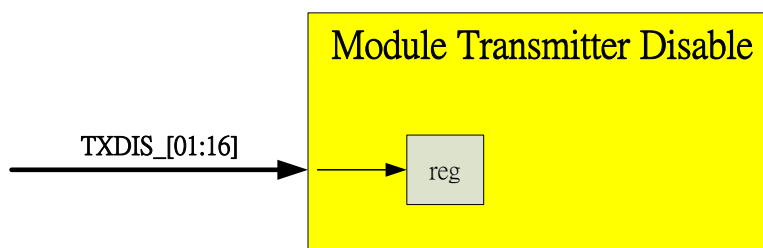
Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	MPL4_SFP63_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 51	MPL4_SFP62_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 54	MPL4_SFP61_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON	MPL4_SFP60_TX_FAULT	R	1	1: SFP Transmit Fault

	Port 55	ULT			0: SFP Transmitter is working well
0	PON Port 58	MPL4_SFP59_TX_FA ULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.14. Offset 0x14 TX_Fault_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	MASK*MPL4_SFP63_ TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 51	MASK*MPL4_SFP62_ TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 54	MASK*MPL4_SFP61_ TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 55	MASK*MPL4_SFP60_ TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 58	MASK*MPL4_SFP59_ TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.15. Offset 0x15 TX_Disable_1 (Read& Write)



The module transmitter disable signal indicates transmitter's output is turned off or not. It is independent of the data inputs.

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON	MPL4_SFP50_TX_DIS	R/W	1	0: Transmitter output is turned on

	Port 52				1: Transmitter output is turned off
6	PON Port 49	MPL4_SFP49_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 48	MPL4_SFP48_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 34	MPL4_SFP47_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 35	MPL3_SFP46_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 38	MPL3_SFP45_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 39	MPL3_SFP44_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 42	MPL3_SFP43_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.16. Offset 0x16 TX_Disable_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	MASK*MPL4_SFP50_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	PON Port 49	MASK*MPL4_SFP49_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	PON Port 48	MASK*MPL4_SFP48_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 34	MASK*MPL4_SFP47_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 35	MASK*MPL3_SFP46_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 38	MASK*MPL3_SFP45_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON	MASK*MPL3_SFP44_TX	R/W	1	1: CPLD can control the TX disable.

	Port 39	_DIS			0: CPLD cannot control the TX disable.
0	PON Port 42	MASK*MPL3_SFP43_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.17. Offset 0x17 TX_Disable_2 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON Port 59	MPL4_SFP58_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	PON Port 62	MPL4_SFP57_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 63	MPL4_SFP56_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 61	MPL4_SFP55_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 60	MPL4_SFP54_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 57	MPL4_SFP53_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 56	MPL4_SFP52_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 53	MPL4_SFP51_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.18. Offset 0x18 TX_Disable_2 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	MASK*MPL4_SFP58_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	PON	MASK*MPL4_SFP57_TX_DIS	R/W	1	1: CPLD can control the TX disable.

	Port 62				0: CPLD cannot control the TX disable.
5	PON Port 63	MASK*MPL4_SFP56_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 61	MASK*MPL4_SFP55_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 60	MASK*MPL4_SFP54_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 57	MASK*MPL4_SFP53_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 56	MASK*MPL4_SFP52_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 53	MASK*MPL4_SFP51_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.19. Offset 0x19 TX_Disable_3 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	MPL4_SFP63_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 51	MPL4_SFP62_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 54	MPL4_SFP61_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 55	MPL4_SFP60_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 58	MPL4_SFP59_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.20. Offset 0x20 TX_Disable_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	MASK*MPL4_SFP63_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 51	MASK*MPL4_SFP62_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 54	MASK*MPL4_SFP61_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 55	MASK*MPL4_SFP60_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 58	MASK*MPL4_SFP59_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.21. Offset 0x21 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	SFP50_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
6	PON Port 49	SFP49_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 48	SFP48_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 34	SFP47_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 35	SFP46_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON	SFP45_LED_ACT	W	1	Steady: No traffic

	Port 38				Blinking: Indicates data traffic on the PON
1	PON Port 39	SFP44_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 42	SFP43_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.22. Offset 0x22 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	SFP58_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
6	PON Port 62	SFP57_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 63	SFP56_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 61	SFP55_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 60	SFP54_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 57	SFP53_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 56	SFP52_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 53	SFP51_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.23. Offset 0x23 SFP_LED_ACT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON	SFP63_LED_ACT	W	1	Steady: No traffic

	Port 50				Blinking: Indicates data traffic on the PON
3	PON Port 51	SFP62_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 54	SFP61_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 55	SFP60_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 58	SFP59_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.24. Offset 0x24 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	SFP50_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 49	SFP49_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
5	PON Port 48	SFP48_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 34	SFP47_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 35	SFP46_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 38	SFP45_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 39	SFP44_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 42	SFP43_LED_LINK_G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.25. Offset 0x25 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	SFP58_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 62	SFP57_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
5	PON Port 63	SFP56_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 61	SFP55_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 60	SFP54_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 57	SFP53_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 56	SFP52_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 53	SFP51_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.26. Offset 0x26 SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	SFP63_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 51	SFP62_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 54	SFP61_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON	SFP60_LED_LINK	W	1	0: PON link up & 1 or more ONTs in service

	Port 55	_G			1: No ONT in service
0	PON Port 58	SFP59_LED_LINK _G	W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.27. Offset 0x27 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	SFP50_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
6	PON Port 49	SFP49_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
5	PON Port 48	SFP48_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
4	PON Port 34	SFP47_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 35	SFP46_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
2	PON Port 38	SFP45_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON Port 39	SFP44_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
0	PON Port 42	SFP43_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.28. Offset 0x28 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	SFP58_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
6	PON Port 62	SFP57_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
5	PON Port 63	SFP56_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

4	PON Port 61	SFP55_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 60	SFP54_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
2	PON Port 57	SFP53_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON Port 56	SFP52_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
0	PON Port 53	SFP51_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.29. Offset 0x29 SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	SFP63_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
3	PON Port 51	SFP62_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
2	PON Port 54	SFP61_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
1	PON Port 55	SFP60_LED_LINK _B	W	1	0: Port disabled 1: Port enabled
0	PON Port 58	SFP59_LED_LINK _B	W	1	0: Port disabled 1: Port enabled

3.30. Offset 0x30 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 52	SFP50_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
6	PON Port 49	SFP49_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

5	PON Port 48	SFP48_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
4	PON Port 34	SFP47_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 35	SFP46_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 38	SFP45_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 39	SFP44_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 42	SFP43_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.31. Offset 0x31 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 59	SFP58_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
6	PON Port 62	SFP57_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
5	PON Port 63	SFP56_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
4	PON Port 61	SFP55_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 60	SFP54_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 57	SFP53_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 56	SFP52_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 53	SFP51_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.32. Offset 0x32 SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:5		Reserved			
4	PON Port 50	SFP63_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
3	PON Port 51	SFP62_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
2	PON Port 54	SFP61_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
1	PON Port 55	SFP60_LED_LINK _R	W	1	0: Fault detected 1: Normal operation
0	PON Port 58	SFP59_LED_LINK _R	W	1	0: Fault detected 1: Normal operation

3.33. Offset 0x33 Reserve (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	FPGA2_CPLD3_RESERVE_B	R/W	1	Reserve from FPGA2 to CPLD3
4	FPGA1_CPLD3_RESERVE_C	R/W	1	Reserve from FPGA1 to CPLD3
3	CPLD3_CPLD2_RESERVE_C	R/W	1	Reserve from CPLD3 to CPLD2
2	CPLD3_CPLD2_RESERVE_B	R/W	1	Reserve from CPLD3 to CPLD2
1	CPLD3_CPLD2_RESERVE_A	R/W	1	Reserve from CPLD3 to CPLD2
0	CPLD3_CPLD1_RESERVE_A	R/W	1	Reserve from CPLD3 to CPLD1

3.34. Offset 0x34 CPU I2C (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD_3_CPU_SDA	R/W		SDA from CPU to CPLD3

0	CPLD_3_CPU_SCL	R/W		SCL from CPU to CPLD3
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3.35. Offset 0x35 LED Stream (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	CPLD3_PON_LED_DATA	R/W		PON LED DATA from FPGA2 to CPLD3
2	CPLD3_PON_LED_CLK	R/W		PON LED CLK from FPGA2 to CPLD3
1	CPLD3_UPLINK_LED_DATA	R/W		Uplink LED DATA from FPGA2 to CPLD3
0	CPLD3_UPLINK_LED_CLK	R/W		Uplink LED CLK from FPGA2 to CPLD3

3.36. Offset 0x36 I2C path select (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	BMC_I2C_SDA_DEVICE_SEL_2	R/W	1	I2C switch MUX 2 1: Allow BMC to access I2C SW 0: Allow CPU to access I2C SW
4	BMC_I2C_SCL_DEVICE_SEL_2	R/W	1	I2C switch MUX 2 1: Allow BMC to access I2C SW 0: Allow CPU to access I2C SW
3	BMC_I2C_SDA_DEVICE_SEL_1	R/W	1	I2C switch MUX 3 1: Allow BMC to access I2C SW 0: Allow CPU to access I2C SW
2	BMC_I2C_SCL_DEVICE_SEL_1	R/W	1	I2C switch MUX 3 1: Allow BMC to access I2C SW 0: Allow CPU to access I2C SW
1				
0				



4.1. Offset 0x01 Power Enable (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved			
1	USB_PWRON_N	R/W	1	0: Disable USB power 1: Enable USB power
2	PS2_ON	R/W	0	0 : PS2 12V output 1 : PS2 12V not output
1	PS1_ON	R/W	0	0 : PS1 12V output 1 : PS1 12V not output
0	12V_CPLD_Power_EN	R/W	1	1: Enable the Hot swap for CPLD. 0: Reset the Hot swap for CPLD.

4.2. Offset 0x02 I2C Path Select (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5				
4				
3				
2				
1	CPU_I2C_SDA_DEVICE_SEL	R/W	1	I2C SWITCH MUX1 1:Allow CPU to access I2C SW 0: Allow BMC to access I2C SW
0	CPU_I2C_SCL_DEVICE_SEL	R/W	1	I2C SWITCH MUX1 1:Allow CPU to access I2C SW 0: Allow BMC to access I2C SW

4.3. Offset 0x03 System Reset_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
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7	USB_RESET_N	R/W	1	1: Normal status 0: Reset USB by SW.
6	2U_FAN_CPLD_RST	R/W	1	1: Normal status 0: Reset 2U FAN CPLD system by SW.
5	CPLD3_TO_CPLD2_RESET	R/W	1	1: Normal status 0: Reset CPLD2 system by SW.
4	CPLD3_TO_CPLD1_RESET	R/W	1	1: Normal status 0: Reset CPLD1 system by SW.
3	PCIE_FPGA2_RESET	R/W	1	1: Normal status 0: Reset FPGA2 system by SW.
2	FPGA2_System_Reset	R/W	1	1: Normal status 0: Reset FPGA2 system by SW.
1	CPLD3_TO_FPGA2_RESET	R/W	1	1: Normal status 0: Reset FPGA2 system by SW.
0	CPLD3_TO_FPGA1_RESET	R/W	1	1: Normal status 0: Reset FPGA1 system by SW.

4.4. Offset 0x04 System Reset_2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			
4	MPL4_SYS_RESET_L	R/W	1	1: Normal status 0: Reset Maple 4 system by SW.
3	MPL3_SYS_RESET_L	R/W	1	1: Normal status 0: Reset Maple 3 system by SW.
2	MPL2_SYS_RESET_L	R/W	1	1: Normal status 0: Reset Maple 2 system by SW.
1	MPL1_SYS_RESET_L	R/W	1	1: Normal status 0: Reset Maple 1 system by SW.
0	MAC_RESET_N	R/W	1	1: Normal status 0: Reset MAC system by SW.

4.5. Offset 0x05 System Reset_3 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4				

3	MPL4_PCIE_RST_L	R/W	1	1: Normal status 0: Reset Maple 4 PCIE by SW.
2	MPL3_PCIE_RST_L	R/W	1	1: Normal status 0: Reset Maple 3 PCIE by SW.
1	MPL2_PCIE_RST_L	R/W	1	1: Normal status 0: Reset Maple 2 PCIE by SW.
0	MPL1_PCIE_RST_L	R/W	1	1: Normal status 0: Reset Maple 1 PCIE by SW.

4.6. Offset 0x06 System Reset_4 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	PCA9548_07_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
6	PCA9548_06_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
5	PCA9548_05_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
4	PCA9548_04_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
3	PCA9548_03_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
2	PCA9548_02_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
1	PCA9548_01_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
0	PCIESW_PERSTN	R/W	1	1: Normal status 0: Reset I2C SW by SW.

4.7. Offset 0x07 System Reset_5 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	PCA9548_x79_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
6	PCA9548_x78_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.

5	PCA9548_x76_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
4	PCA9548_x75_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
3	PCA9548_x74_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
2	PCA9548_x73_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
1	PCA9548_09_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.
0	PCA9548_08_RESET	R/W	1	1: Normal status 0: Reset I2C SW by SW.

4.8. Offset 0x08 System Reset_6 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:3	Reserved			
2	PCA9548_x82_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
1	PCA9548_x81_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.
0	PCA9548_x80_RESET_N	R/W	1	1: Normal status 0: Reset I2C SW by SW.

4.9. Offset 0x09 Power present (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:3	Reserved			
2	PS2_PRESENT	R/W	1	0 : PS2 Present 1 : PS2 Not present
1	PS1_PRESENT	R/W	1	0 : PS1 Present 1 : PS1 Not present
0	MAIN_BOARD_POWER_PRESENT_5	R/W	0	0: Main board power off 1: Main board power on

4.10. Offset 0x10 Power Alert (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	PS2_PDB_ALERT	R/W		0: PS2 POWER Operate 1: PS2 POWER Shut Down
2	PS1_PDB_ALERT	R/W		0: PS1 POWER Operate 1: PS1 POWER Shut Down
1	PS2_AC_ALERT	R/W		0: PS2 POWER Fail 1: PS2 POWER Good
0	PS1_AC_ALERT	R/W		0: PS1 POWER Fail 1: PS1 POWER Good

4.11. Offset 0x11 Power Good (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	OTDR_B_PG	R/W	1	0: OTDR_B 2.9V Power Fail 1: OTDR_B 2.9V Power Good
2	OTDR_A_PG	R/W	1	0: OTDR_A 2.9V Power Fail 1: OTDR_A 2.9V Power Good
1	PS2_12V_PG	R/W	1	0: PS2 12V Power Fail 1: PS2 12V Power Good
0	PS1_12V_PG	R/W	1	0: PS1 12V Power Fail 1: PS1 12V Power Good

4.12. Offset 0x12 USB Power fault (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	USB_PWRFLT_N	R/W	1	0: USB power fault (overcurrent, over-

				temperature, or reverse-voltage conditions) 1: Normal operation
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4.13. Offset 0x13 Interrupt (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved			
6	2U_FAN_INT_L	R/W	0	0: No interrupt from 2U FAN 1: Receive Interrupt from 2U FAN
5	FAN_INT_L	R/W	0	0: No interrupt from 1U FAN 1: Receive Interrupt from 1U FAN
4	MPL4_INTERRUOT	R/W	0	0: No interrupt from MPL4 1: Receive Interrupt from MPL4
3	MPL3_INTERRUOT	R/W	0	0: No interrupt from MPL4 1: Receive Interrupt from MPL4
2	MPL2_INTERRUOT	R/W	0	0: No interrupt from MPL4 1: Receive Interrupt from MPL4
1	MPL1_INTERRUOT	R/W	0	0: No interrupt from MPL1 1: Receive Interrupt from MPL1
0	MAC_CPLD_INT_L	R/W	0	0: No interrupt from MAC 1: Receive Interrupt from MAC

4.14. **Offset 0x11 FAN Idle (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	2U_FAN_IDLE	R/W	1	
0	FAN_IDLE	R/W	1	

4.15. Offset 0x12 ID Button (Read only)

Bit	Name	R/W	Reset Value	Description
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7:1	Reserved			
0	ID_BUTTON	R	1	1: Non-push the push button of front panel 0: Push the push button of front panel

4.16. Offset 0x13 MAC Reset (Read only)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	RESET_MAC88470	R	0	1: Reset MAC request form CPU 0: Normal operation

4.17. Offset 0x14 BMC I2C (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD_3_BMC_SDA	R/W		SDA from BMC to CPLD3
0	CPLD_3_BMC_SCL	R/W		SCL from BMC to CPLD3

4.18. Offset 0x15 Interrupt Stream (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD3_TO_FPGA2_INTERRUPT_DATA	R/W		Interrupt DATA from CPLD3 to FPGA2
0	CPLD3_TO_FPGA2_INTERRUPT_CLK	R/W		Interrupt CLK from CPLD3 to FPGA2

4.19. Offset 0x16 System LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
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7	UID_LED	R/W	1	Front Panel UID LED
6	AIRFLOW_LED_B	R/W	1	Front Panel FAN status Blue LED
5	AIRFLOW_LED_R	R/W	1	Front Panel FAN status Red LED
4	AIRFILTER_LED	R/W	1	Front Panel AIRFLTER LED
3	POWER2_LED_G	R/W	1	Front Panel Power 2 STATUS Green LED
2	POWER2_LED_R	R/W	1	Front Panel Power 2 STATUS Red LED
1	POWER1_LED_G	R/W	1	Front Panel Power 1 STATUS Green LED
0	POWER1_LED_R	R/W	1	Front Panel Power 1 STATUS Red LED

4.20. Offset 0x17 System LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	ALARM_LED_B	R/W	1	Front Panel Alarm STATUS Blue LED
6	ALARM_LED_G	R/W	1	Front Panel Alarm STATUS Green LED
5	ALARM_LED_R	R/W	1	Front Panel Alarm STATUS Red LED
4	STATE_LED_B	R/W	1	Front Panel State STATUS Blue LED
3	STATE_LED_G	R/W	1	Front Panel State STATUS Green LED
2	STATE_LED_R	R/W	1	Front Panel State STATUS Red LED
1			0	
0			0	